Electronic Version
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Claims

[c1] 1.A serial flash-memory chip comprising:

a flash-memory array of electrically-erasable programmable read-only memory (EEPROM) cells;

row and column decoders for selecting EEPROM cells in the flash-memory array for reading, writing, or erasing in response to a flash address;

a serial-bus interface to a serial bus connected to pins of the serial flash-memory chip, for transmitting and receiving serial data over the serial bus;

a serial engine, coupled to the serial-bus interface, for converting serial data from the serial bus to parallel data;

an internal controller, coupled to the serial engine, for responding to flash commands sent over the serial bus in request packets, and for generating completion packets that are sent over the serial bus in response to the flash commands; and

data buffers, coupled between the flash-memory array and the internal controller, for buffering data read from the EEPROM cells in response to the internal controller decoding a read flash command in a read-request packet, the data being loaded into a data payload of a

completion packet;

wherein the internal controller programs data into the EEPROM cells through the data buffers in response to a program flash command in a write-request packet received over the serial bus,

whereby the serial flash-memory chip has a serial-packet interface for commands, address, and data.

[c2] 2.The serial flash-memory chip of claim 1 wherein the write-request packet contains a program flash command;

wherein the internal controller generates a vendor-defined message packet with a completion status for transmission over the serial bus after the EEPROM cells have been programmed, the vendor-defined message packet being part of a different serial-bus transaction than the write-request packet that initiated programming of the EEPROM cells;

whereby the vendor-defined message packet is generated after completion of a program operation.

[c3] 3.The serial flash-memory chip of claim 2 wherein the write-request packet contains a cache-program flash command;

wherein the internal controller generates a message-request packet for transmission over the serial bus before completion of programming the EEPROM cells, the mes-

sage-request packet being part of a same serial-bus transaction for the write-request packet that initiated programming of the EEPROM cells.

[c4] 4.The serial flash-memory chip of claim 3 wherein an erase flash operation is initiated by the internal controller receiving an erase flash command in a vendor-defined message packet received over the serial bus;
wherein the internal controller generates a second message packet for transmission over the serial bus after completion of the erase flash operation, the second message packet being part of a different serial-bus transaction than the vendor-defined message packet that initiated erasing of the EEPROM cells;
whereby the second message packet is generated after completion of an erase flash operation.

[c5] 5.The serial flash-memory chip of claim 2 wherein the internal controller resets the serial flash-memory chip in response to a reset-flash command in the vendor-defined message packet received over the serial bus.

[c6] 6.The serial flash-memory chip of claim 5 wherein the internal controller generates a completion packet with a copy of a status register as a data payload in response to a configuration-read-request packet received over the serial bus;

wherein the status register contains status flags or an identifier of the serial flash-memory chip.

[c7] 7.The serial flash-memory chip of claim 5 wherein each packet sent or received over the serial bus contains a header having a type field and a format field that define a type and a format for each packet,
wherein packet types include the read-request packet, the write-request packet, and a message packet sent to the serial flash-memory chip, and the completion packet and a message packet generated by the internal controller.

[c8] 8.The serial flash-memory chip of claim 7 wherein the write-request packet contains a data payload containing data to program into the EEPROM cells, but the read-request packet contains no data payload;
wherein the completion packet generated in response to the read-request packet contains a data payload containing data read from the EEPROM cells.

[c9] 9.The serial flash-memory chip of claim 8 wherein the read-request packet contains the flash address that is sent to the row and column decoders to select data in the EEPROM cells for reading;
wherein the write-request packet contains the flash address that is sent to the row and column decoders to se-

lect EEPROM cells for programming.

[c10] 10.The serial flash-memory chip of claim 2 wherein the serial bus is a Universal-Serial-Bus (USB), a Peripheral Component Interconnect (PCI) Express bus, a Firewire IEEE 1394 bus, a Serial ATA bus, or a Serial Attached Small-Computer System Interface bus.

[c11] 11.The serial flash-memory chip of claim 2 wherein the serial bus is a Peripheral Component Interconnect (PCI) Express bus that has pairs of differential lines including a transmit differential pair and a receive differential pair.

[c12] 12.The serial flash-memory chip of claim 3 wherein the flash address has lower address bits that indicate when a flash command conveyed by the packet is the cache-program flash command, the program flash command, or a copy-back-program flash command;
wherein the lower address bits are not necessary to uniquely locate EEPROM cells within the flash-memory array,
whereby lower address bits in the flash address select a type of write operation.

[c13] 13.The serial flash-memory chip of claim 2 wherein the internal controller comprises a microcontroller, a state machine, or a controller logic block.

[c14] 14.A flash-memory chip with a serial-packet interface comprising:

a serial-bus interface to an external serial bus that transfers serial packets that include a memory-read-request packet, a memory-write-request packet, a configuration-read-request packet, and an input message packet input to the flash-memory chip, and a completion packet and an output message packet output from the flash-memory chip;

flash memory means for storing data in non-volatile flash-memory cells;

controller means, coupled to the flash memory means and to the serial-bus interface, for performing operations identified by commands in the serial packets, the operations including:

reading data from the flash memory means at a flash address included in a header for the memory-read-request packet to generate a data payload for the completion packet;

writing data to the flash memory means at the flash address included in a header for the memory-write-request packet, the data being sent in a data payload in the memory-write-request packet;

reading a status from a configuration register identified by a header in the configuration-read-request packet to

generate a data payload for the completion packet;
erasing a block of memory in the flash memory means in response to an erase indicator in a header in the input message packet and generating the output message packet once erasing is completed; and
resetting the flash-memory chip in response to a reset indicator in a header in the input message packet,
whereby operations are performed by the flash-memory chip in response to commands in serial packets received over the external serial bus include generation of completion packets with the data payload read from the flash memory means.

[c15] 15.The flash-memory chip of claim 14 further comprising:
transaction-layer means, coupled to the controller means, for generating the completion packet by attaching a completion-packet header to the data payload, and for generating the output message packet by generating a message header indicating a completion status;
data-link layer means, coupled to the controller means, for encapsulating a transaction-layer packet generated by the controller means by adding a sequence number to a header and a checksum to generate a data-link packet; and
physical-layer means, in the serial-bus interface, for

framing the data-link packet for transmission over the external serial bus.

[c16] 16.The flash-memory chip of claim 15 wherein the serial-bus interface connects to the external serial bus that is a bi-directional serial bus with an incoming pair of differential signal lines and an outgoing pair of differential signal lines.

[c17] 17.The flash-memory chip of claim 15 wherein the serial-bus interface comprises no more than a plurality of four signal pins, the plurality of four signal pins being only pins to carry address, commands, and data to the flash-memory chip during normal operation;
wherein the flash-memory chip is in a package having ten or fewer external pins.

[c18] 18.A Peripheral Component Interconnect (PCI) Express flash-memory chip comprising on a single semiconductor substrate:
a flash memory array of non-volatile electrically-erasable programmable read-only memory (EEPROM) cells;
address decoders, receiving a flash address, the address decoders selecting a subset of the EEPROM cells for reading, writing, or erasing;
a high-voltage generator for generating elevated voltages above a power-supply voltage for programming

and erasing the EEPROM cells;

data buffers for storing data being written to the EEP-ROM cells;

a command register receiving a flash command;

control logic, responsive to the flash command in the command register, for controlling reading, writing, and erasing of the EEPROM cells;

a serial interface to external pins of the PCI Express flash-memory chip that connect to an external serial bus, the serial interface having a physical layer;

wherein the external serial bus is a PCI Express serial bus having differential data lines that carry data serially;

a controller, connected between the serial interface and the command register and data buffers, the controller comprising:

a data-link layer that encapsulates transaction-layer packets for transmission over the external serial bus af-ter framing by the physical layer;

a transaction layer that generates headers to attach to data payloads to generate the transaction-layer packets;

read operation means, responsive to a memory-read-request packet received over the external serial bus having a header with the flash address, for sending a read command to the command register and sending the flash address to the address decoders, and transferring data read from the EEPROM cells from the data buffers to

the transaction layer as a data payload, the transaction layer attaching the data payload to a header to generate a completion packet with the read data, the completion packet being sent over the external serial bus as a response to the memory-read-request packet;

program operation means, responsive to a memory-write-request packet received over the external serial bus having a header with the flash address, for sending a write command to the command register and sending the flash address to the address decoders, and transferring data write from a data payload of the memory-write-request packet to the data buffers for writing to the EEPROM cells;

erase operation means, responsive to a message packet received over the external serial bus having a header with an erase indicator, for sending an erase command to the command register, and generating a message packet for transmission over the external serial bus once the EEPROM cells have been erased; and

reset operation means, responsive to a message packet received over the external serial bus having a header with a reset indicator, for sending a reset command to the control logic to reset the control logic and to reset the controller,

whereby operations indicated by commands in serial packets received over the external serial bus are exe-

cuted and data is returned in data payloads of serial packets.

[c19] 19.The PCI Express flash-memory chip of claim 18 wherein the program operation means further comprises:

slow write means for generating a message packet for transmission over the external serial bus after writing to the EEPROM cells is completed, the message packet containing a completion status;

cached write means for generating a message packet for transmission over the external serial bus before writing to the EEPROM cells is completed;

wherein the read operation means further comprises:

register-read means, responsive to a configuration-read-request packet received over the external serial bus having a header with a register address, for transferring data read from a register to the transaction layer as a data payload, the transaction layer attaching the data payload to a header to generate a completion packet with the register data, the completion packet being sent over the external serial bus as a response to the configuration-read-request packet.

[c20] 20.The PCI Express flash-memory chip of claim 18 further comprising:

packed-write means, coupled to the controller, for read-

ing mask bytes in the data payload of the memory-write-request packet to determine locations of EEPROM cells for writing with data in data bytes in the data payload of the memory-write-request packet,
whereby the data payload is packed according to the mask bytes.

[c21] 21.The PCI Express flash-memory chip of claim 18 further comprising:
an expansion serial interface to expansion external pins of the PCI Express flash-memory chip that connect to an external expansion serial bus, the expansion serial interface having a physical layer;
wherein the expansion external serial bus is a PCI Express serial bus having differential data lines that carry data serially to a second PCI Express flash-memory chip;